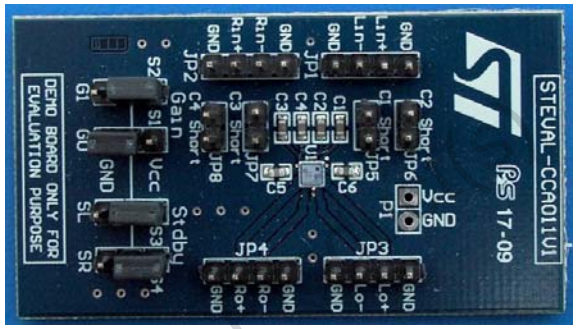
STEVAL-CCA011V1

Filter-free stereo 2x2.5 W Class-D audio power amplifier demonstration board based on the TS2012FC

Data brief

Features

- Operating range from V_{CC} = 2.5 V to 5.5 V
- Dedicated standby mode active low for each channel
- Output power per channel: 1.15 W @5 V or 0.63 W @ 3.6 V into 8 Ω with 1% THD+N max
- Output power per channel: 1.85 W @5 V into 4 Ω with 1% THD+N max
- Output short-circuit protection
- Four gain select settings: 6, 12, 18, 24 dB
- Low current consumption
- PSRR: 63 dB typ @ 217 Hz with 6 dB gain
- Fast start-up phase: 8 ms
- Thermal shutdown protection
- RoHS compliant



STEVAL-CCA011V1

Description

This demonstration board is based on TS2012FC that is a fully differential Class-D stereo power amplifier able to drive up to 1.15 W into an 8 Ω load at 5 V per channel.

It achieves better efficiency compared to typical Class-AB audio amps.

The device has four different gain settings that use two digital pins: G0 and G1. Pop and click reduction circuitry provides low on/off switch noise while allowing the device to start within 8 ms.

Two standby pins (active low) allow each channel to be switched off independently.

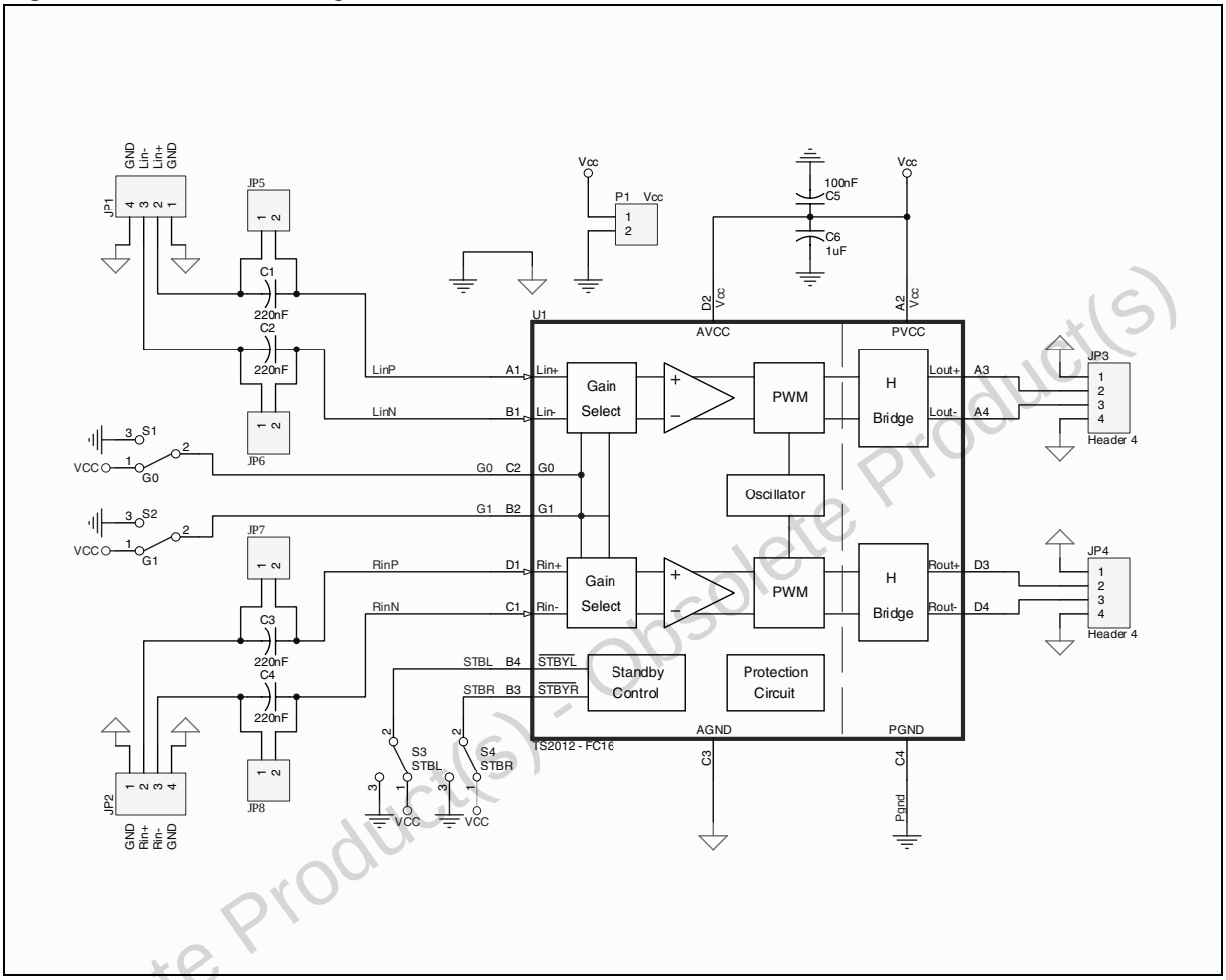
The TS2012FC also integrates output short-circuit protection and thermal shutdown protection and it is available in a 16-bumps Flip-Chip package.

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1 Circuit schematics

Figure 1. Schematic diagram



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Table 1. Component list for the demonstration board

Designation	Quantity	Description
C1, C2, C3, C4	4	220 nF/16 V, SMD ceramic capacitor, 0603
C5	1	100 nF/16 V, SMD ceramic capacitor, 0603
C6	1	1 µF/16 V, SMD ceramic capacitor, 0603
P1, JP5, JP6, JP7, JP8	5	2-pin header 2.54 mm pitch
S1, S2, S3, S4	4	3-pin header 2.54 mm pitch
JP1, JP2, JP3, JP4	4	4-pin header 2.54 mm pitch
U1	1	TS2012EIJT

2 Demonstration board layout

The following figures depict the top view and layers of the demonstration board.

Figure 2. PCB top layer

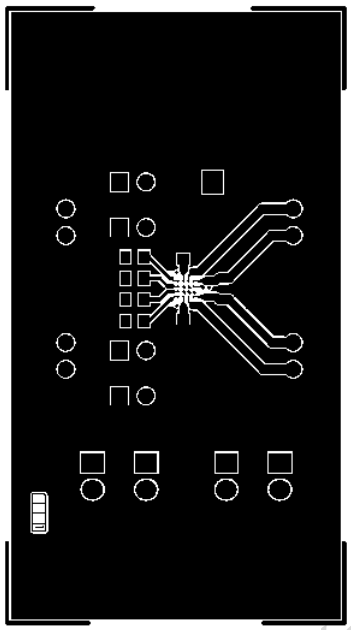


Figure 3. PCB middle layer 1

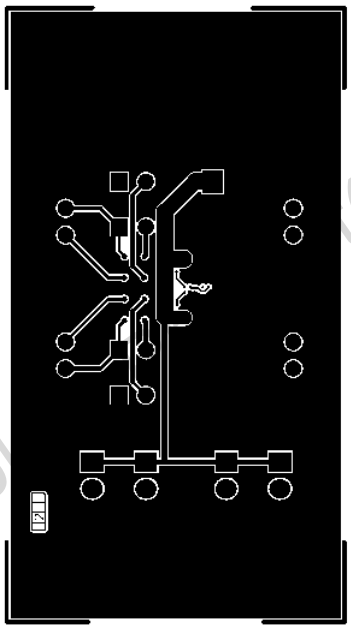


Figure 4. PCB middle layer 2

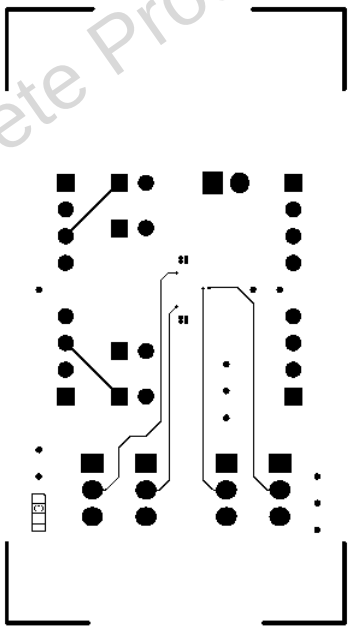
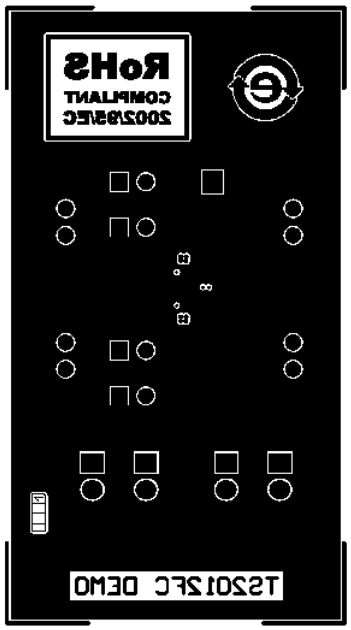
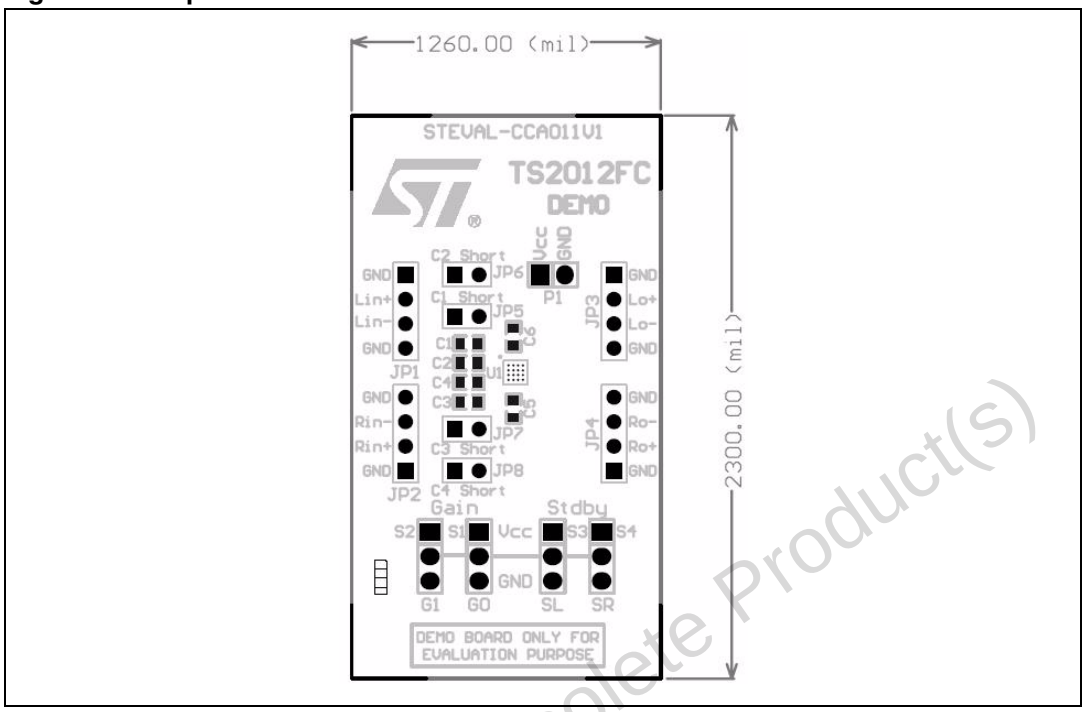


Figure 5. PCB bottom layer



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Figure 6. Top view and dimensions of the demonstration board



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3 Revision history

Table 2. Document revision history

Date	Revision	Changes
03-Jun-2009	1	Initial release.

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